

### DESCRIPTION:

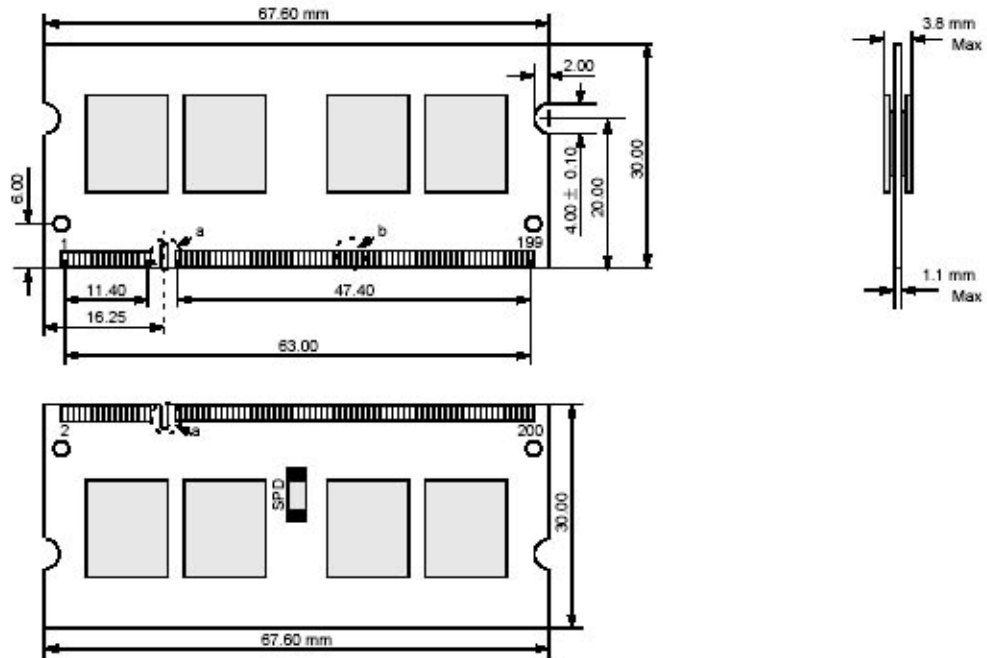
This document describes Aplus 128M x 64-bit 2GB DDR2-800 CL5 SDRAM (Synchronous DRAM) memory module. The components on this module include sixteen 128M x 8-bit (4Banks) DDR2-800 SDRAM in FBGA packages. This 200-pin DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

### FEATURES:

- JEDEC standard 1.8V  $\pm$  0.1V Power supply
- All inputs and outputs SSTL\_1.8 compatible
- Max clock Freq: 400Mhz
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe (DQS)
- Differential clock inputs (CK and CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 5 (clock)
- Programmable Burst length (4,8)
- Programmable Burst type (sequential & interleave)
- Timing Reference: CL-tRCD-tRP (5-5-5)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- OCD ( Off-chip driver impedance adjustment )
- ODT ( On-die termination )
- Serial presence detect with EEPROM

### PERFORMANCE:

|                                 |                              |
|---------------------------------|------------------------------|
| Clock Cycle Time ( tCK )        | 2.5ns (min.) /8ns (max.)     |
| Row Cycle Time ( tRC )          | 51.5ns (min.)                |
| Refresh Row Cycle Time ( tRFC ) | 105ns (min.)                 |
| Row Active Time ( tRAS )        | 39ns (min.) /70,000ns (max.) |
| Operating Temperature           | 0°C ~ 85°C                   |
| Storage Temperature             | -55°C ~ +100°C               |



DETAIL a

DETAIL b

