

DESCRIPTION:

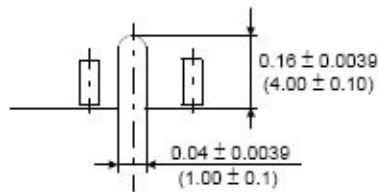
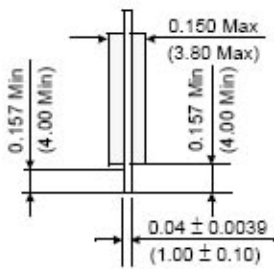
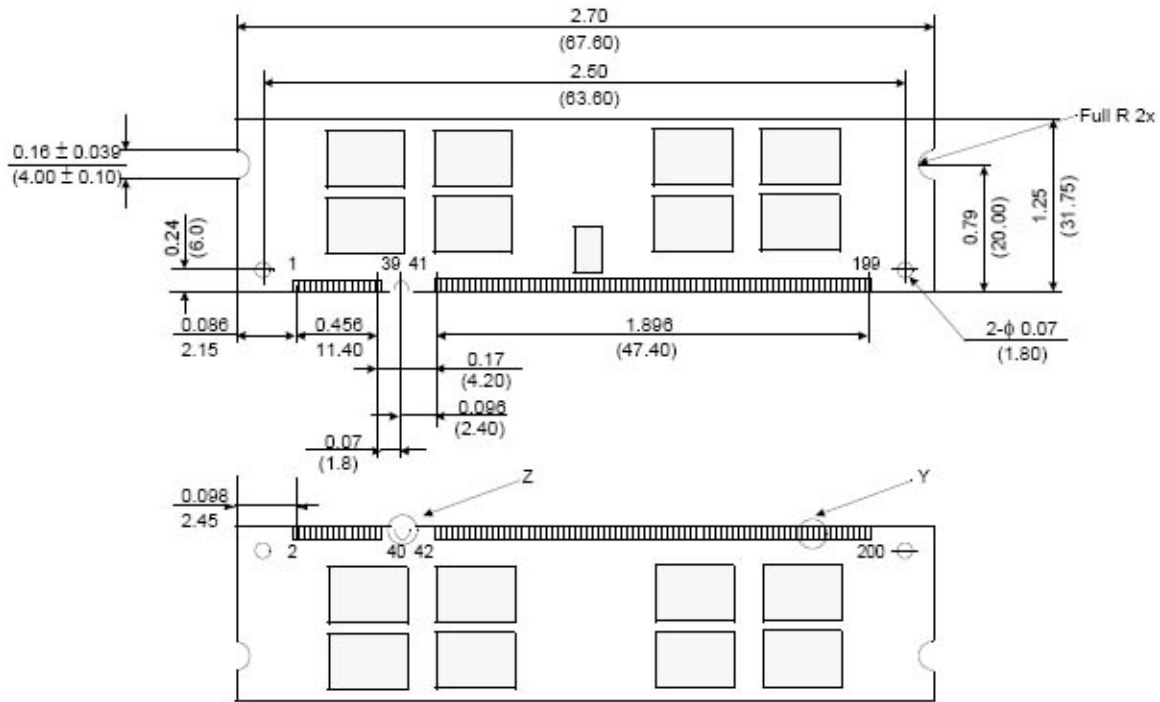
This document describes Aplus 128M x 64-bit 1G DDR266 CL2.5 SDRAM (Synchronous DRAM) memory module. The components on this module include sixteen 64M x 8-bit (4 Bank) DDR266 SDRAM in FBGA packages. This 200-pin SO-DIMM uses gold contact fingers and requires +2.5V. The electrical and mechanical specifications are as follows:

FEATURES:

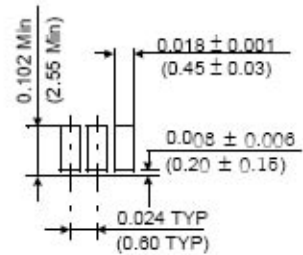
- Power supply: Vdd: 2.5V ± 0.2V , Vddq: 2.5V ± 0.2V
- All inputs and outputs SSTL_2 compatible
- Max clock Freq: 133Mhz
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe (DQS)
- Differential clock inputs (CK and CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2.5 (clock)
- Programmable Burst length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Timing Reference: CL-tRCD-tRP (2.5-3-3)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect with EEPROM

PERFORMANCE:

Clock Cycle Time (tCK)	7.5ns (min.) /12ns (max.)
Row Cycle Time (tRC)	65ns (min.)
Refresh Row Cycle Time (tRFC)	75ns (min.)
Row Active Time (tRAS)	45ns (min.) /120,000ns (max.)
Power Dissipation	16W
Operating Temperature	0°C to 70 °C
Storage Temperature	-55°C to +150 °C



Detail Z



Detail Y