APLUS TECHNOLOGY

DDR2 533/667 FULLY BUFFERED DIMM 4GB 256Mx4

DESCRIPTION:

This document describes Aplus 512M x 72-bit 4GB DDR2 SDRAM (Synchronous DRAM) ECC memory module The components on this module include thirty-six 256M x 4-bit (4Banks) DDR2 SDRAM in FBGA packages. This 240-pin Fully Buffered DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

FEATURES:

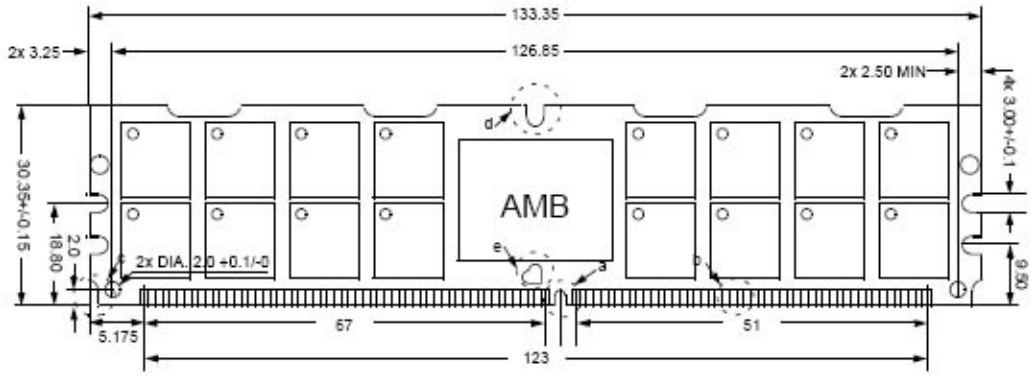
JEDEC standard Double data rate2
1.8V ± 0.1V Power supply for DRAM VDD/VDDQ
1.5V +0.075/-0.045V Power supply for AMB VCC
3.3V ± 0.3V Power supply for VDDSPD
All inputs and outputs are compatible with SSTL_1.8 interface
Host interface and AMB component industry standard compliant
High-speed differential point-to-point link at 1.5volt
Link transfer rate 3.2Gb/s, 4.0Gb/s
Programmable Burst length 4/8 with both sequential and interleave mode
8192 refresh cycles / 64ms
OCD (Off-chip driver impedance adjustment)
ODT (On-die termination)
MBIST IBIST test functions
Serial presence detect with EEPROM

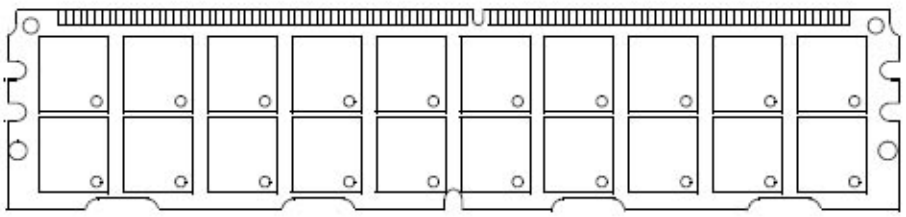
DDR2 DRAM Speed

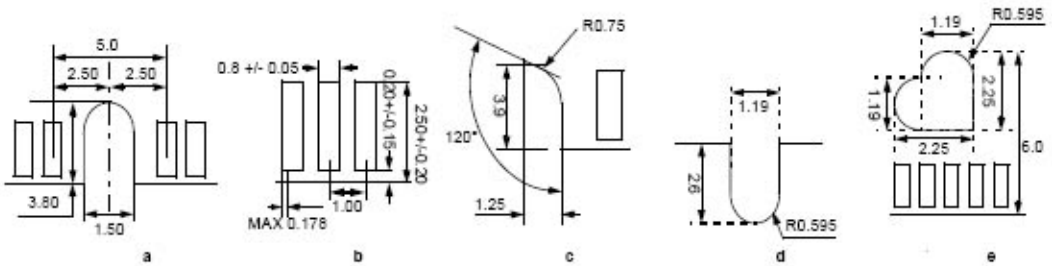
DDR2-667 667Mbps CL-tRCD-tRP (5-5-5)
DDR2-533 533Mbps CL-tRCD-tRP (4-4-4)

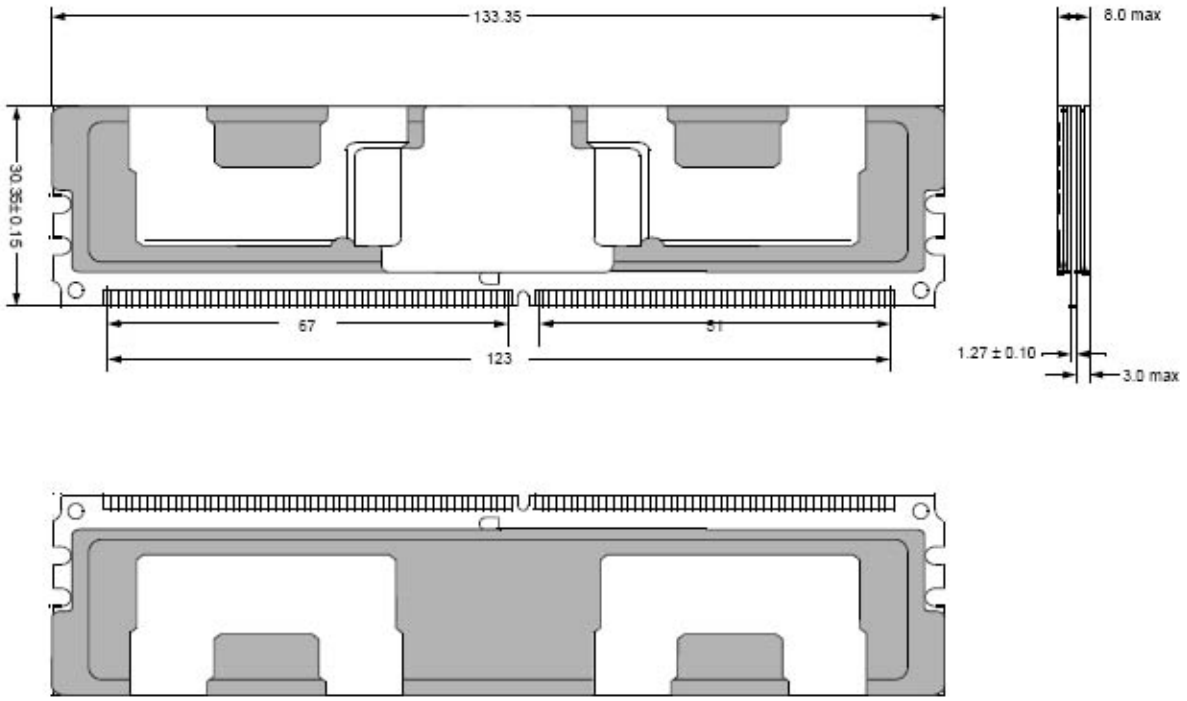
PERFORMANCE:

Clock Cycle Time (tCK) CL(5) 3ns (min.) /8ns (max.)
Clock Cycle Time (tCK) CL(4) 3.75ns (min.) /8ns (max.)
Row Cycle Time (tRC) 60ns (min.)
Refresh Row Cycle Time (tRFC) 105ns (min.)
Row Active Time (tRAS) 45ns (min.)
Operating Temperature 0℃ ~ 95℃
Storage Temperature -55℃ ~ +100℃


133.35
126.85
2x 3.25
2x 2.50 MIN
4x 3.00+/-0.1
30.35+/-0.15
18.80
2.0
2x DIA. 2.0 +0.1/-0
AMB
d
e
a
b
9.50
5.175
67
51
123




5.0
2.50
2.50
3.80
1.50
a
0.8 +/- 0.05
0.20+/-0.15
2.50+/-0.20
1.00
MAX 0.178
b
R0.75
3.9
120°
1.25
c
1.19
2.6
R0.595
d
1.19
R0.595
1.19
2.25
2.25
6.0
e


133.35
8.0 max
30.35±0.15
67
51
123
1.27 ± 0.10
3.0 max